Hot Carrier and Soft Breakdown Effects On VCO Performance

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Abstract — ***This* paper systematically investigates the hot carrier and soft-breakdown induced performance degradation in a CMOS voltage-controlled oscillator used in phase locked loop frequency synthesizers. After deriving the closed-form equations to predict phase noise and VCO gain, we relate VCO RF performance such as phase noise, tuning range and gain of VCO subject to electrical stress. The circuit degradations predicted by analytical model equations are verified by SpectraRF simulation using parameters extracted from the experimental data of 0.16 μm CMOS technology.**

I. Introduction

As CMOS device sizes shrink, the channel electric field becomes higher and the hot carrier (HC) effect becomes more significant [1]. When the oxide is scaled down to less than 3 nm, soft-breakdown (SBD) often takes place [2], [3], [4]. As a result, oxide trapping and interface generation cause long term performance drift and related reliability problems in devices and circuits.

Voltage controlled oscillator (VCO) is the most important circuit in a phase locked loop frequency synthesizer. It dominates almost all spectral purity performance of a frequency synthesizer. It is desirable for a VCO to generate low noise signal with sufficient output power, wide tuning range, and high stability. However, the VCO performance is very sensitive to the variation of device parameters. The experimental results show that device performance will be degraded significantly subject to HC stress and SBD [5]. Therefore, it is anticipated that the VCO performance is degraded by hot electron stress and oxide soft breakdown.

In this paper, the device performance drifts due to HC and SBD are examined experimentally by measuring threshold voltage, mobility and transconductance before and after stress for 0.16 μm CMOS technology. Phase noise, tuning range, and gain degradations of a CMOS 5-stage ring oscillator VCO are systematically evaluated.

II. Device Degradation Due To HC And SBD

To examine the HC and SBD effects, gate and substrate currents are measured respectively with the device overstress to reduce the characterization time. The impact of HC and SBD can be characterized as the degradation of major device parameters such as threshold voltage and mobility. The combination effect of HC and SBD is indicted by experimental results.

The devices tested are 0.16 μm technology nMOSFETs. The oxide thickness is 2.4 nm and the gate width is 50 μm. Many transistors are tested to verify the statistical variance. The wafer is tested with the Cascade 12000 Probe Station and Agilent 4156B Precision Semiconductor Parameter Analyzer. The gate and drain voltages used for overstress are at 2.6 volts and then measured at gate and drain voltages of 0.85 and 1.5 volts, respectively for reasonable operating condition. The source and bulk are grounded. For N-channel devices, the measured threshold voltage increases with stress time because of electron trapping, and the measured mobility decreases due to the increase of interface state generation. This is verified by the degradation of the extracted parameters of BSIM3v3 model. From Figure 1, the threshold voltage increases by 40% and the mobility decreases by 45% after stress.

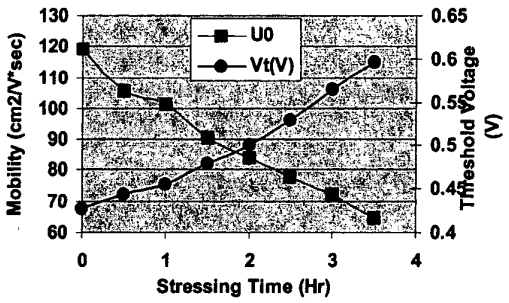

Fig. 1 Threshold voltage and mobility degradation

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The drain current and transconductance decrease after stress due to the degradation of threshold voltage and mobility. The drain current degradation is shown in Fig. 2.

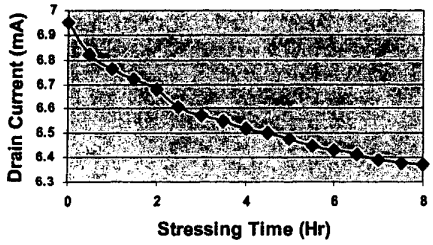

Fig. 2 Drain current degradation due to HC and SBD

The SBD and HC effects also degrade the RF parameters of CMOS devices. The same wafer is stressed and probed with Cascade 12000 Probe Station and the RF parameters are examined using Agilent 8510C Network Analyzer. The device s-parameters are measured and cutoff frequency and maximum frequency of oscillation are extracted before and after stress. From the experimental data, S_{11} and S_{21} degrade significantly after stress, and the cutoff frequency and maximum frequency of oscillation decrease greatly as well. The cutoff frequency degradation is shown in Fig. 3.

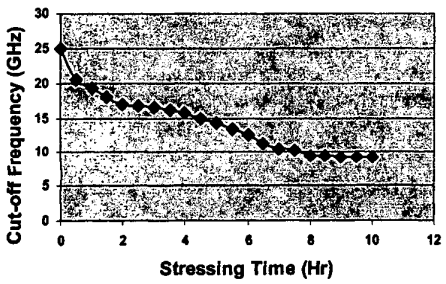

Fig. 3 Cutoff frequency degradation subject to stress

III. Analytical Derivation

The major parameters for VCOs are phase noise, tuning range and gain. In order to predict the degradation of VCO major parameters due to HC and SBD effects, closed form analytical equations for these parameters as a function of threshold voltage and mobility are derived. A 5-stage ring VCO composed of 5 fully differential delay stages is examined. As shown in Fig. 4, each delay cell consists of NMOS differential pairs with PMOS resistive loads. The gate voltage V_G is controlled carefully by a replica biasing circuit (not shown here) so that the PMOS transistors are working in the linear region and the voltage swing is kept constant. The major concerns here are the device channel thermal noise sources and their impact on the VCO timing jitter [6]. Flicker noise is not considered here because it will be filtered out by the PLL bandwidth at low frequency.

The NMOS and PMOS transistors are working in the saturation and linear regions, respectively, whose channel thermal noise current power spectral densities are given by:

$$\overline{i_n^2} = 4kT\gamma_n g_m \Delta f \quad (1)$$

$$\overline{i_n^2} = 4kT\gamma_p g_d \Delta f \quad (2)$$

where g_m is the transconductance and γ_n is the noise factor of the NMOS transistors and g_d is the drain-to-source transconductance and γ_p is the noise factor of the PMOS transistors.

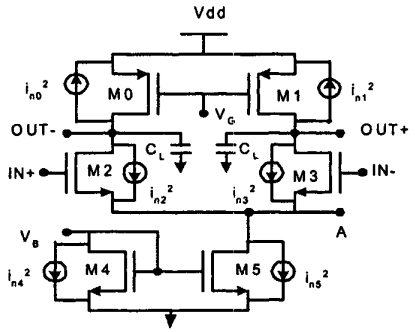

Fig. 4 Delay cell with channel thermal noise sources

By analyzing the impact of every device channel thermal noise source on the output noise, including the time-varying effect and inter-stage amplification, the output noise of single delay cell in terms of major device parameters is given by:

$$\overline{V_n^2} = \frac{kT}{2}\frac{G^2\alpha^2}{C_L} \quad (3)$$

where G is the gain of the delay cell, α is the noise factor given by:

$$\alpha^2 = 2\gamma_p + 2\gamma_n G\{1+[\sqrt{\frac{X_1}{2}}(1+X_2)-1](1+\frac{4t_D}{\tau_D}+\frac{8t_D^2}{\tau_D^2})e^{-\frac{4t_D}{\tau_D}}\} \quad (4)$$

and X_1 is the size ratio of M5 and M3, X_2 is the size ratio of M4 and M3, t_D is the time delay of a single delay cell and τ_D is time constant for output capacitance load.

The timing jitter for single delay stage is given by

$$\sigma_D^2 = \frac{kT}{2}\frac{G^2}{I_{ss}^2}\alpha^2 C_L \tag{5}$$

For a n-stage ring oscillator, the output frequency is $f_0 = \frac{1}{2nt_D}$, and the output timing jitter is $\sigma_{f_0}^2 = 2n\sigma_D^2$ given by

$$\sigma_{f_0}^2 = \frac{kT}{2}\frac{G}{I_{SS}(V_{gs}-V_{Tn})}\frac{\alpha^2}{f_0} \tag{6}$$

The output phase noise of a ring oscillator is thus

$$L\{f_m\} = \frac{f_0}{f_m^2}\frac{\sigma_{f_0}^2}{T_0^2} = (\frac{f_0}{f_m})^2 \frac{kTG\alpha^2}{\mu \cdot C_{OX}(\frac{W}{L})_5 (V_{gs3}-V_{Tn})(V_{gs5}-V_{Tn})^2} \tag{7}$$

For a phase locked loop, the oscillator frequency is controlled by the bias current corresponding to the bias voltage V_B. The VCO gain corresponds to a small change of output frequency caused by the control voltage with respect to phase difference between the reference frequency and the $1/N$ of the VCO frequency. The differential control circuit is shown in Fig. 5. The input is from the differential output of charge pump and loop filter.

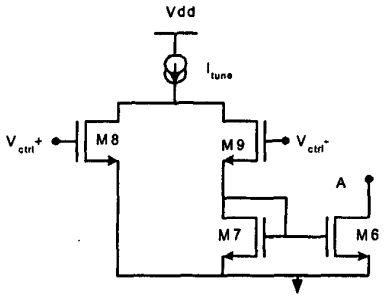

Fig. 5 A control circuit

The VCO gain is given by

$$G_{VCO} = \frac{\partial f_0}{\partial V_{ctrl}} \cong \frac{\partial f_0}{\partial I_t} g_m X_t \tag{8}$$

where I_t is the tuning current and X_t is the size ratio of M6 and M7.

IV. VCO Degradations Subject To Stress

Using the analytical equations derived in Sec. III, the VCO performance degradation due to HC and SBD effects are examined. A 5-stage ring oscillator is considered. First, the wafer of 0.16 um CMOS process is stressed on the Cascade 12000 Probe Station and then measured at Agilent 8510C Network Analyzer. The measured parameters are used in both the model file for Cadence SpectraRF simulation and our analytical model. The predicted phase noise change due to HC and SBD effects is shown in Fig. 6, and the simulation results are shown in Fig. 7. It is clear that the phase noise increases by about 6 dB after stress. Good agreement between the model predictions and simulation results are obtained.

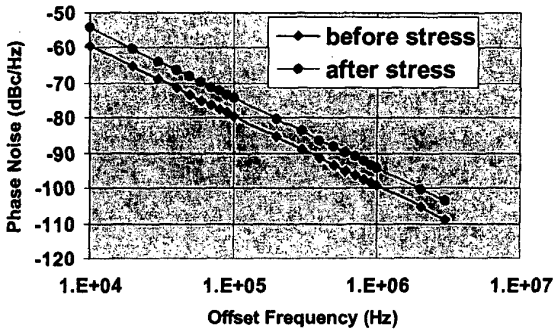

Fig. 6 Predicted phase noise versus offset frequency

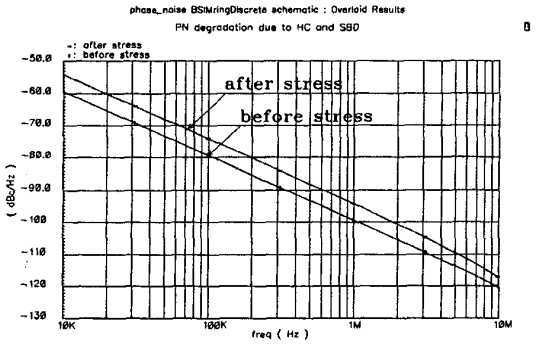

Fig. 7 SpectraRF simulation results

The VCO tuning range changes dramatically after stress. From Figure 8, the VCO center frequency drifts about 55MHz, and the tuning range decreases 20%, from 344MHz to 274MHz after about 2.25 hour stress.

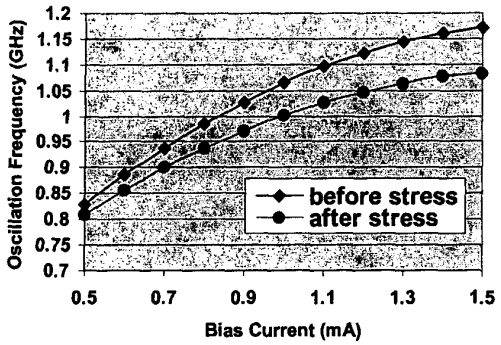

Fig. 8 Tuning range degradation

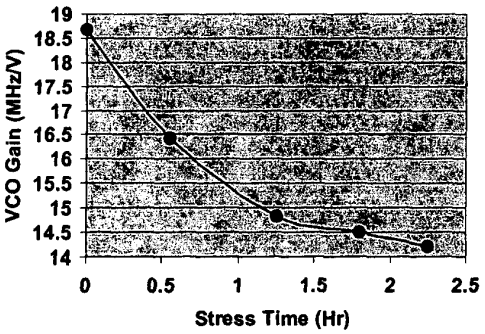

Fig. 9 VCO gain degradation

From Fig. 9 the VCO gain is reduced by 24% after 2.25 hours stress. The above figures show that the HC and SBD induced effects degrade the VCO performance dramatically. After stress, the phase noise will increase, and the center frequency, the tuning range and the gain will decrease. It is expected that the VCO performance degradation would affect the performance of the PLL, then the whole receiver performance. The increased phase noise would degrade the selectivity of the receiver and the lowered tuning range and gain will impact the locking time and stability of the receiver.

The normalized VCO phase noise and gain degradations as a function of change of threshold voltage and mobility are derived in (9) and (10).

$$\frac{\Delta L\{f_m\}}{L\{f_m\}} = \frac{1}{(1+\frac{\Delta\mu}{\mu})(1-\frac{\Delta V_{Tn}}{V_{gs3}-V_{Tn}})(1-\frac{\Delta V_{Tn}}{V_{gs5}-V_{Tn}})^2} - 1 \qquad (9)$$

$$\frac{\Delta G_{VCO}}{G_{VCO}} = (1+\frac{\Delta\mu}{\mu})(1-\frac{\Delta V_{Tn}}{V_{gs}-V_{Tn}}) - 1 \qquad (10)$$

It is clear from (9) and (10) that $V_{gs} - V_{Tn}$ for each delay cell should be chosen as large as possible to reduce the degradation due to HC and SBD effects, but needs to be small enough to guarantee the gain greater than one to sustain oscillation. These results would be helpful for designing more reliable RF circuits.

V. SUMMARY

The analytical equations to predict VCO performance degradation subject to hot electron stress and oxide soft breakdown are derived. Device parameters of 0.16 um CMOS technology were measured before and after stress. The analytical model predictions of VCO performance are compared with SpectreRF simulation. The phase noise increases and VCO gain and tuning range decrease with respect to stress time. Good agreement between the model predictions and simulation results is obtained.

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